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A −10 to −20-V Inverting Buck-Boost Drive GaN Driver With Sub-1-μA Leakage Current V_{th} Tracking Technique for 20-MHz Depletion-Mode GaN Metal–Insulator–Semiconductor High-Electron-Mobility Transistors

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***Abstract*— This article proposes an inverting buck-boost drive (IBBD) gallium nitride (GaN) driver, which directly drives depletion-mode GaN (D-GaN) metal–insulator–semiconductor high-electron-mobility transistor (MIS-HEMT). In the proposed driver fabricated with a 0.5-μm CMOS process, the V_{th} tracking technique can reduce switching loss and minimize the leakage current of D-GaN MIS-HEMT to sub-1 μA. To suppress the electromagnetic interference (EMI) caused by the ringing voltage at drain of the GaN switch when reducing from 22 to 1.9 V, a Miller plateau (MP) detector and an EMI suppression frequency controller (ESFC) are also applied. With the slew rate (SR) control and fast-level shifter, the maximum switching frequency can reach up to 20 MHz, and dV_{DS}/dt can be regulated at 120 V/ns. In addition, the power saving mode of IBB converter and accurate ultralow power (ULP) under voltage lockout (UVLO) are proposed to reduce the quiescent current to 580 nA during standby mode, thereby enhances light load efficiency. The peak efficiency is as high as 95.8% and chip areas are 5.1 and 6.6 mm^2.**

***Index Terms*— Gallium nitride (GaN), Miller plateau (MP) voltage, ultralow quiescent current, V_{th} tracking.**

I. Introduction

THE normally-on depletion-mode GaN (D-GaN) metal–insulator–semiconductor high-electron-mobility transistors (MIS-HEMTs) [1], [2] have the advantages of low gate leakage current, low parasitic capacitance, and lower temperature coefficient (TC) of ON-resistance ($R_{\text{DS(ON)}}$) compared

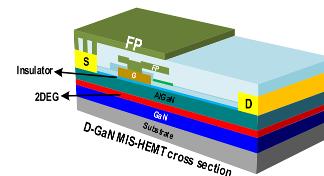

Fig. 1. Cross section of the D-GaN MIS-HEMT with FP.

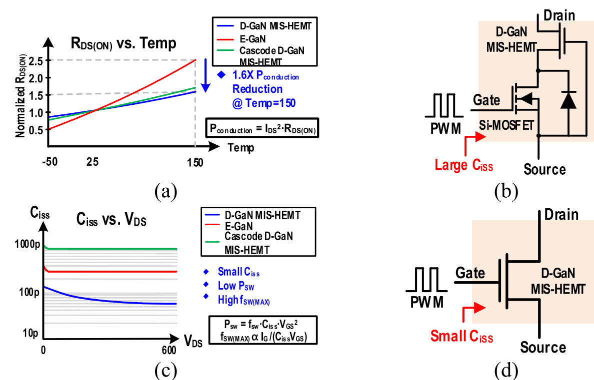

Fig. 2. (a) Normalized on resistance versus temperature of different GaN transistors. (b) Structure of cascode D-GaN MIS-HEMT. (c) Input capacitance verses drain–source voltage of different GaN transistors. (d) Structure of the proposed IBBD D-GaN MIS-HEMT.

with enhancement-mode GaN (E-GaN) [3]–[7]. Fig. 1 shows the cross section of the D-GaN MIS-HEMT. Due to the insulator layer, the gate leakage current can be reduced to hundreds of pA, and the lower TC of $R_{\text{DS(ON)}}$ can reduce the conduction loss down to 1.6 times at 150 °C, as shown in Fig. 2(a).

However, the gate-to-source voltage (V_{GS}) needs to be less than its threshold voltage V_{th} (−10 to −20 V) to turn off the D-GaN MIS-HEMT. To ensure normally off operation, in state-of-the-arts, D-GaN MIS-HEMT is cascaded in series with low-voltage (LV) Si-MOSFET as a cascode structure [8]–[13], as shown in Fig. 2(b). Although the turn-on threshold voltage becomes positive due to the

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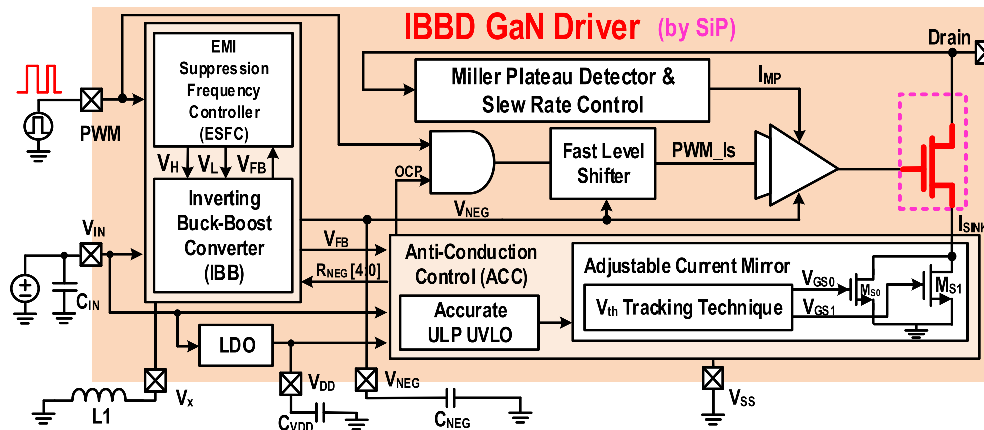

Fig. 3. Structure of the proposed ACC technique.

pulsewidth modulation (PWM) signal applied to the gate of the LV Si-MOSFET, the cascode structure will cause the following problems. First, the input capacitance (C_{iss}) of LV Si-MOSFETs is normally a few nanofarads. The larger C_{iss}, compared to that of D-GaN, will increase the switching loss and limit the maximum switching frequency [$f_{\text{SW(MAX)}}$], as shown in Fig. 2(c). Second, the LV Si-MOSFET may suffer from avalanche problems [14], [15] due to junction capacitance mismatch during turn-off transition, which will cause additional power loss and reliability concerns. Although adding the extra capacitor in parallel with Si-MOSFET can prevent avalanche problems [14], the undesirable extra capacitor may induce extra turn-off loss and increase chip areas. Third, when the body diode of Si-MOSFET switches from forward voltage to reversed voltage, the large reverse recovery current flows through the diode [8]–[13], which will cause extra power loss. To solve the problems mentioned above, this article proposed an inverting buck-boost drive (IBBD) D-GaN MIS-HEMT, as shown in Fig. 2(d). The GaN switch control signal is sent to the gate of D-GaN MIS-HEMT directly. Reducing C_{iss} can effectively reduce switching loss, and thus, high switching frequency can be achieved. C_{iss} of cascade D-GaN, in Fig. 2(c), is about 1000 pF, while C_{iss} of D-GaN MOS-HEMT is only 100 pF. The gate-to-source voltage V_{GS} swing of cascade D-GaN is about 5 V, while the V_{GS} swing of D-GaN MOS-HEMT is about 13 V. Consequently, the switching power loss can have a 32% reduction. The efficient IBBD D-GaN MIS-HEMT driver can be applied to ac to dc applications, such as Flyback, power factor converter (PFC), and *LLC* converter designs.

In this article, the IBBD GaN driver with V_{th} tracking technique is proposed to reduce switching loss and prevent leakage current. This article is organized as follows. Section II introduces the architecture of the proposed IBBD GaN driver. Section III shows the detailed circuit implementation, including anticonduction control (ACC) technique, Miller plateau (MP) detector and slew rate (SR) control, inverting buck-boost converter with electromagnetic interference (EMI) suppression frequency controller (ESFC), fast-level shifter, and accurate ultralow-power (ULP) undervoltage-lockout (UVLO). In Section IV, the measurement results for the test chip and the comparison table are given. Finally, Section V presents the conclusion.

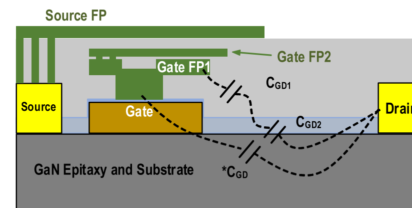

Fig. 4. Miller capacitance (C_{GD}) verses drain–source voltage with different FP designs.

II. Proposed IBBD GaN Driver

Fig. 3 shows the block diagram of the proposed IBBD GaN driver, which directly turns on and off the D-GaN MIS-HEMT by 0 V and V_{th}, respectively. To prevent excessive negative voltage driving from causing the current collapse, the field plate (FP) structure [16], [17] in D-GaN MIS-HEMT is applied to reduce the gate trap effect under high electric fields, as shown in Fig. 1. Compared with cascode D-GaN MIS-HEMT, by applying the PWM signal to the gate of D-GaN MIS-HEMT, switching loss can be greatly reduced to achieve high efficiency and high switching frequency [$f_{\text{SW(MAX)}} \propto I_G / C_{\text{iss}} V_{\text{GS}}$].

In addition, to alleviate the trapping problems in the high-voltage D-GaN MIS-HEMT designs, the proposed FP can affect the electric field distribution of the GaN layer while restraining the device from withstanding large voltages on the drain (D) terminal [18]. The original parasitic capacitance ($*C_{\text{GD}}$) effect can be modified by the FP to smaller series capacitances C_{GD1} and C_{GD2}, as shown in Fig. 4. Moreover, this article uses the FP implementation in different metal layers, such as Gate FP1, Gate FP2, and Source FP in the D-GaN HMT design. In Fig. 5, the blue curve is the $*C_{\text{GD}}$ of D-GaN MIS-HEMT without FP. Once Gate FP1 is inserted, C_{GD1} is parallel with $*C_{\text{GD}}$ when V_{DS} is at an LV level, so a large parasitic capacitance is generated. However, when V_{DS} rises, C_{GD1} and C_{GD2} will have a series effect, so C_{GD} drops in one step when V_{DS} increases to a high value, as indicated

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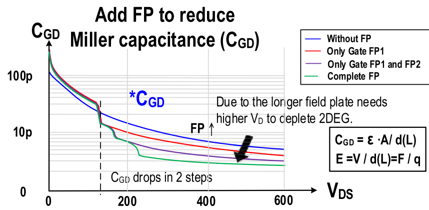

Fig. 5. Diagram of miller capacitance (C_{GD}) verses drain–source voltage with different FP designs.

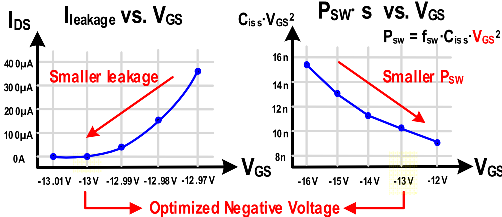

Fig. 6. Leakage current and switching loss at different gate drive voltages.

by the red curve. Similarly, the second layer of Gate FP2 can make C_{GD} to have a second step down, as shown in the purple curve. Lastly, by inserting the source FP, the parasitic capacitance effects is improved at a higher V_{DS} and the electric field strength is reduced, as shown in the green curve. As a result, C_{GD} drops with a step when V_{DS} increases to a higher value in Fig. 5. Thus, due to low C_{GD}, D-GaN MIS-HEMT is more suitable for high-frequency operations.

However, V_{th} of different D-GaN MIS-HEMTs varies due to different processes and different V_{DS} values. Too much negative turn-off voltage ($V_{\mathrm{GS}} = -14$ V in Fig. 6) will cause large gate swing voltage and switching loss, while less negative turn-off voltage ($V_{\mathrm{GS}} = -12$ V in Fig. 6) will not turn off D-GaN MIS-HEMT completely and cause a large leakage current. Thus, the gate drive voltage of D-GaN MIS-HEMT needs to be adjusted according to different GaN switches. The proposed ACC uses the V_{th} tracking technique to detect V_{th}, and the ON-chip inverting buck-boost (IBB) converter generates a negative voltage (V_{NEG}) that is less than V_{th} to reduce the leakage current of GaN and the switching loss in normal operation. When the switching frequency increases, the fast V_{GS} swing may cause a larger dV_{DS}/dt, which leads to serious EMI problems [19], [20]. Therefore, the MP detector is used to accurately detect the MP voltage (V_{MP}) to avoid the ringing of the drain voltage and suppress EMI. Moreover, the ESFC can adjust the switching frequency of the IBB converter to synchronize with the PWM signal to further suppress EMI. With low C_{iss}, well-controlled dV_{DS}/dt through the SR control and fast-level shifters for reducing control signal delay, the maximum switching frequency is up to 20 MHz. To reduce the power consumption of the GaN driver in standby mode, the power saving mode of the IBB converter and accurate ULP UVLO is proposed to reduce the quiescent current and guarantee high accuracy at the same time.

III. Circuit Implementations

A. ACC Technique

The architecture of the proposed ACC, as shown in Fig. 7, consists of three function blocks, including accurate ULP UVLO, adjustable current mirror, and low offset sense amplifier. The accurate ULP UVLO can check the voltage level of the supply voltage V_{IN}, logic control supply voltage V_{DD}, and the negative gate drive voltage V_{NEG}. To avoid leakage current during power-on, the accurate ULP UVLO can decide whether or not to turn on the LV Si-MOSFET M_{S0} and M_{S1} according to the level of three voltage signals. Moreover, the low quiescent current of the accurate ULP UVLO can reduce power consumption in normal operation mode and thus improve the efficiency. The adjustable current mirror can adjust the size of sensing MOSFET to achieve more accurate current sensing. The high current sensing ratio is adopted during V_{th} tracking mode to precisely sense the small leakage current of D-GaN MIS-HEMT. On the other hand, the low current sensing ratio is adopted during normal operation mode to detect large current for overcurrent protection. The low offset amplifier is used to reduce the channel length modulation effect of sensing MOSFET to further improve the accuracy of current sensing.

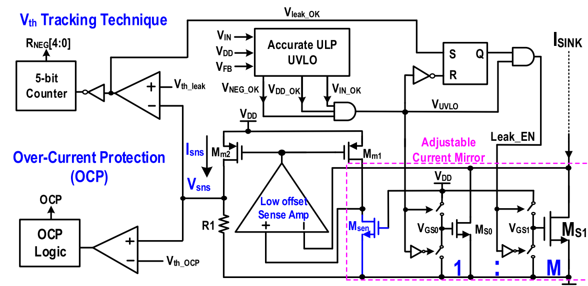

Fig. 7. Structure of the proposed ACC.

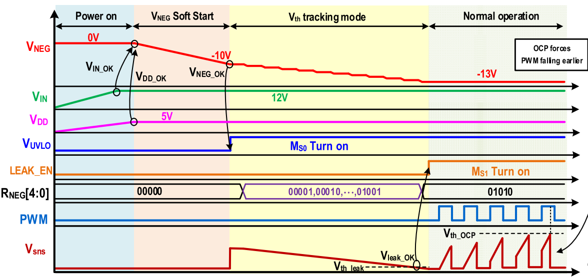

Fig. 8. Timing diagram of the power-on and V_{th} tracking process of the proposed ACC technique.

Fig. 8 shows the operation of the ACC technique, which can be divided into four time zones. During power-on, the accurate ULP UVLO can check whether V_{IN} and V_{DD} rise to the target level 12 and 5 V, respectively. Then, the soft-start procedure of V_{NEG} turns off M_{S0} and M_{S1} to avoid any leakage current of the D-GaN MIS-HEMT. When V_{NEG} reaches a predetermined value, the soft start procedure is ended to trigger the V_{th} tracking mode.

The V_{th} tracking mode can determine how negative the value of V_{NEG} requires to reach in order to completely turn off D-GaN MIS-HEMT. Once V_{th} tracking mode is triggered, the small size M_{S0} in series with D-GaN MIS-HEMT is turned on to monitor the leakage current. By setting the current mirror

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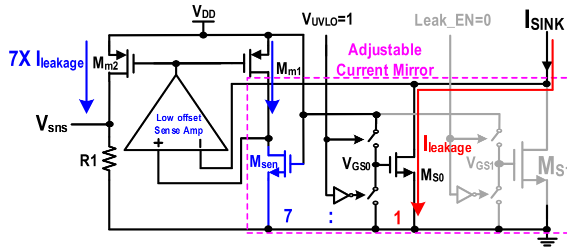

Fig. 9. Operation of adjustable current mirror in the V_{th} tracking technique.

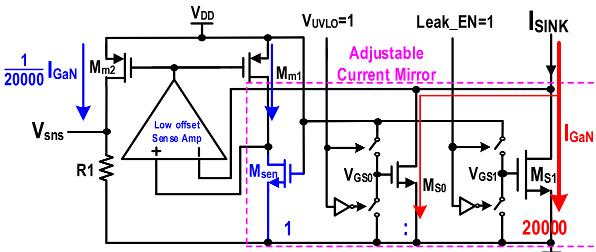

Fig. 10. Operation of adjustable current mirror in normal operation.

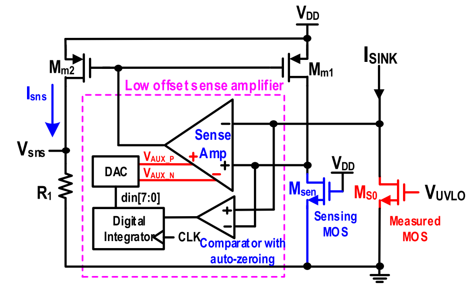

Fig. 11. Architecture of the low offset sense amplifier.

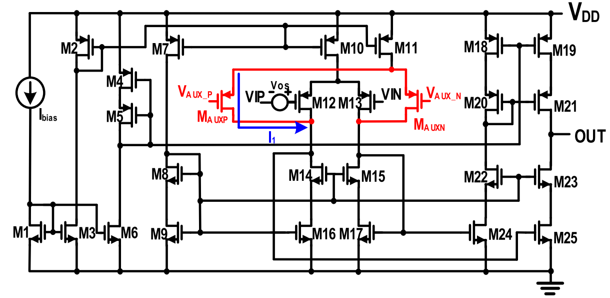

Fig. 12. Sense amplifier with an offset cancellation.

ratio M_{S0}:M_{sen} to 1:7, the small leakage current of D-GaN MIS-HEMT is amplified and monitored by the sensing signal V_{sns}, as shown in Fig. 9. V_{NEG} can be calibrated to be more negative through the 5-bit counter $R_{\text{NEG}}[4:0]$. Once V_{sns} is less than the leakage threshold voltage $V_{\text{th_leak}}$, the signal LEAK_EN is set to logic high to indicate the end of V_{th} tracking. In normal operation, M_{S0} and M_{S1} are always turned on to avoid avalanche effect and reverse recovery current problems. Meanwhile, V_{sns} generated by the current mirror (M_{S1}:M_{sen}), as shown in Fig. 10, represents the drain current of the GaN switch, which can be used to compare with the overcurrent threshold voltage $V_{\text{th_OCP}}$ to achieve overcurrent protection.

In the V_{th} tracking process, the leakage current of D-GaN MIS-HEMT is detected through the adjustable current mirror. The current of sensing MOSFET depends on the drain–source voltage V_{DS}. To ensure the accuracy of the sensing current, V_{DS} of sensing MOSFET is controlled to be equal to the measured MOSFET by the sense amplifier. However, the input offset of the sense amplifier will vary due to process, supply voltage, and temperature (PVT) variation and will result in the mismatch of V_{DS} voltage between sensing MOSFET and measured MOSFET. This will affect the accuracy of the V_{th} tracking process and cause the D-GaN MIS-HEMT to have large leakage current. Therefore, this article proposes the low offset amplifier to improve the precision of current sensing.

The architecture of the low offset sense amplifier is shown in Fig. 11. The offset cancellation circuits are composed of a low offset comparator, digital integrator, and digital to analog converter (DAC). With the autozeroing technique, the low offset comparator can reach ultralow offset voltage and is connected to the inputs of the sense amplifier to detect the offset voltage. The comparison results of the offset voltage will be sent to a digital integrator and generate the 8-bit correction signal din[7:0]. Through the DAC, a digital correction signal will be transferred into the analog domain. The signals $V_{\text{AUX_P}}$ and $V_{\text{AUX_N}}$ will be sent to the sense amplifier and generate a correction current to cancel the offset voltage of the sense amplifier.

Fig. 12 shows the circuit of the sense amplifier. The drain voltages of M_{sen} and M_{S0} are sent to the input pair VIP and VIN, respectively, and generate the output signal OUT to control the current source M_{m1} in Fig. 11, making the drain voltage of M_{sen} and M_{S0} the same. To cancel the offset between M_{12} and M_{13}, the auxiliary input pair M_{AUXP} and M_{AUXN} is used. If a positive offset voltage V_{OS} occurs at VIP, the correction signal $V_{\text{AUX_P}}$ from the offset cancellation circuit will decrease to generate the correction current I_1 to compensate the offset, thereby improving the accuracy of current sensing. To detect the offset voltage of the sense amplifier, the comparator uses the autozeroing technique to reach ultralow offset. Thus, the proposed sense amplifier with an offset cancellation circuit can sense the offset of the sense amplifier precisely and reach ultralow offset.

B. MP Detector and SR Control

Fig. 13 shows the structure of the MP detector and SR control, and their operation timing diagram is presented in Fig. 14. In the SR control, a small value capacitor C1 is used to sense the derivative of V_{DS} to generate I_{C1} as (1). Then, the SR signal V_{SR} can be derived in (2) by mirroring I_{C1} to the resistor R_{ERR}

$$I_{\text{C1}} = dV_{\text{DS}}/dt \cdot \text{C1} \quad (1)$$

$$V_{\text{SR}} = (I_{\text{C1}} + I_{\text{bias}}) \cdot R_{\text{ERR}} + V_{\text{ref,MP}}. \quad (2)$$

To control the SR, V_{SR} is regulated within the SR hysteresis window, which is composed of lower and upper bounds, $V_{\text{ref,SR}}$

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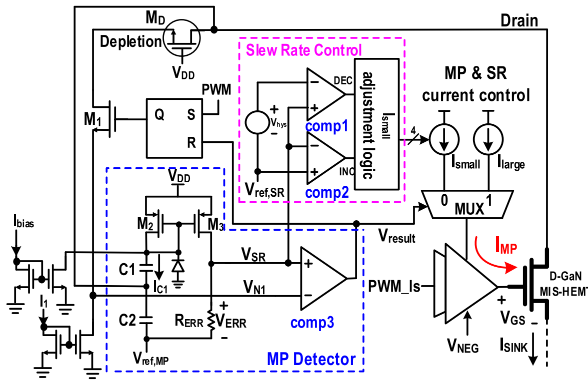

Fig. 13. Architecture of SR control and MP detector.

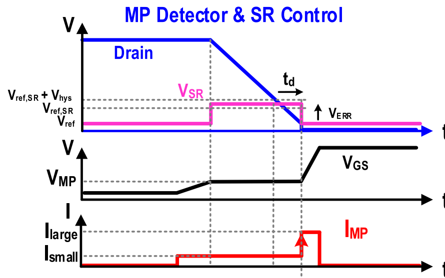

Fig. 14. Operation timing diagram of MP detector and SR control.

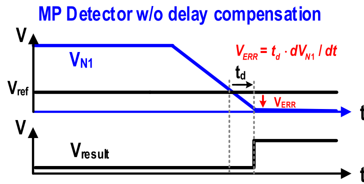

Fig. 15. MP detector without delay compensation.

and $V_{hys}+V_{ref,SR}$, respectively. Through the comparison results produced by the comparators "comp1" and "comp2," the decrease and increase signals "DEC" and "INC," respectively, can decrease and increase the small gate charging current I_{small}. A well-controlled SR of V_{DS} can reduce EMI.

In order to accurately detect the end of the MP period, the drain voltage of D-GaN is detected to derive the switching status where the N-channel depletion transistor M_D is used to withstand the high drain voltage to protect the MP detector. When the drain voltage is higher than $V_{DD}+|V_{th,MD}|$, M_D will keep V_{N1} at about $V_{DD}+|V_{th,MD}|$. On the other hand, when the drain voltage is lower than $V_{DD}+|V_{th,MD}|$, M_D will be fully turned on to let V_{N1} directly track the drain voltage. Therefore, V_{N1} can be compared with V_{SR} by the comparator "comp3." If V_{N1} is still higher than V_{SR}, I_{small} is used to avoid the ringing of the drain voltage and alleviate the EMI problem. Contrarily, when V_{N1} is lower than V_{SR}, V_{result} will be high, which indicates the end of the MP period. Meanwhile, the MP and SR current control will select a large gate charging current I_{large} to accelerate the turn-on process.

The comparator "comp3" in Fig. 13 has its propagation delay t_d, as shown in Fig. 15, which causes a response that

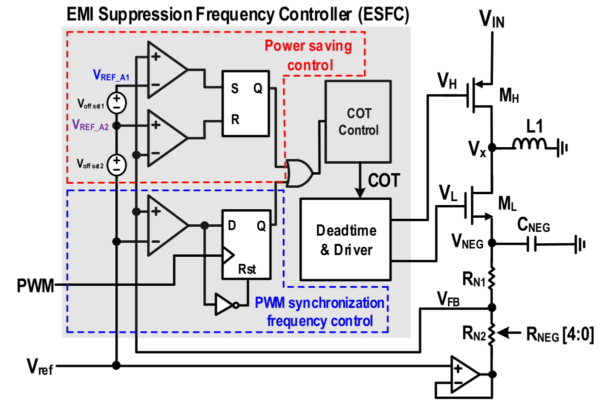

Fig. 16. Architecture of IBB converter with ESFC.

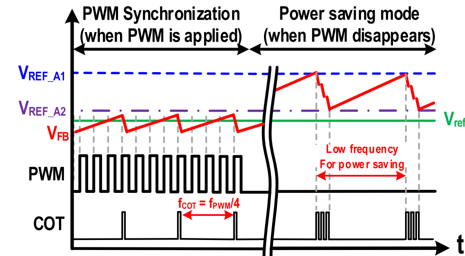

Fig. 17. Operation timing diagram of IBB converter with ESFC and f_{COT} synchronizes with f_{PWM} when there are PWM inputs.

occurs when V_{N1} is equal to $V_{ref,MP}-V_{ERR}$ and not $V_{ref,MP}$, thereby inducing the MP detector to detect the error of MP. To alleviate the propagation delay error in (3), an offset voltage V_{ERR} in (4) is added by flowing the I_{C1} and ON-chip basic bias current I_{bias} to the resistor R_{ERR}, so that the comparison result of V_{N1} and V_{SR} can occur earlier to reduce the effect of t_d for a precise MP detection, where R_{ERR} can be determined by (5)

$$\text{Error due to propagation delay} = t_d \cdot dV_{N1}/dt \quad (3)$$

$$V_{ERR} = (dV_{DS}/dt \cdot C1 + I_{bias}) \cdot R_{ERR} \quad (4)$$

$$R_{ERR} = t_d/[C1 + I_{bias}/(dV_{DS}/dt)]. \quad (5)$$

C. Inverting Buck-Boost Converter With EMI Suppression Frequency Controller

To further suppress EMI, the ESFC is proposed to synchronize the constant on-time switching frequency f_{COT} of the IBB converter with the PWM frequency f_{PWM}. The structure of ESFC is shown in Fig. 16. The ESFC can be divided into two parts, PWM synchronization frequency control and power saving control. In normal operation, through PWM synchronization frequency control, V_{NEG} can be charged at the rising edge of PWM when the energy of V_{NEG} is insufficient ($V_{FB} > V_{ref}$), as shown in Fig. 17. By using this control, the switching frequency f_{COT} of the IBB converter is synchronized with f_{PWM}, which can further assist with the EMI suppression.

When the loading system switches into standby mode, the IBB converter will enter power saving mode to enhance light load efficiency by reducing switching frequency. Fig. 17 shows

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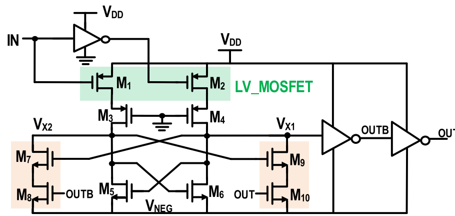

Fig. 18. Architecture of fast-level shifter.

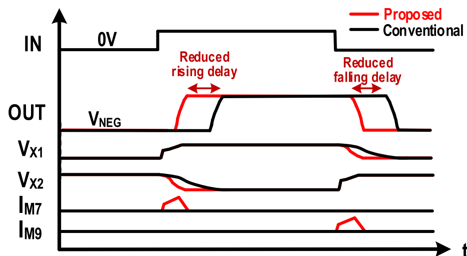

Fig. 19. Operation timing diagram of fast-level shifter.

the operation timing diagram of the power saving mode. In power saving mode, IBB converter will be activated to charge V_{NEG} when it is insufficient, which is when V_{FB} is larger than V_{REF_A1}. Until the energy of V_{NEG} is sufficient, which is when V_{FB} is smaller than V_{REF_A2}, the converter will shut down to stop charging. Therefore, V_{NEG} is finally regulated in the hysteretic window between V_{REF_A1} and V_{REF_A2} by reducing the switching frequency to enhance the light load efficiency. During the absence of f_{PWM}, the IBB converter can regulate V_{NEG} with a minimum energy until the next input of f_{PWM}.

D. Fast-Level Shifter

In order to increase the maximum switching frequency, the fast-level shifter is proposed to reduce the delay in GaN gate driving signal. The structure of the fast-level shifter is shown in Fig. 18. The input pair within the structure of the fast-level shifter M_1 and M_2 is LV MOSFESTs, which can reduce the delay due to small input capacitance, and the HV MOSFETs M_3 and M_4 are applied to withstand high voltage. Moreover, the extra two pull-down paths (M_7–M_8) and (M_9–M_{10}) controlled by V_{X1} and V_{X2}, respectively, are applied to further reduce the delay. As shown in Fig. 19, when the rising edge of the input signal occurs, the rising voltage V_{X1} will conduct M_7, and the pull-down current I_{M7} will increase to rapidly pull down V_{X2} and reduce the rising delay. On the contrary, when the falling edge occurs, the rising voltage V_{X2} will conduct M_9, and the pull-down current I_{M9} will increase to rapidly pull down V_{X1} and reduce the falling delay. In conclusion, with the fast-level shifter, the rising and falling delay in GaN gate driving signal can be further reduced by 70% due to the LV MOSFESTs input pair and extra pull-down current I_{M7} and I_{M9}. Furthermore, the reduced delay can further increase the maximum switching frequency.

E. Accurate ULP UVLO

The architecture of the proposed accurate ULP UVLO is shown in Fig. 20. To reduce the power consumption of

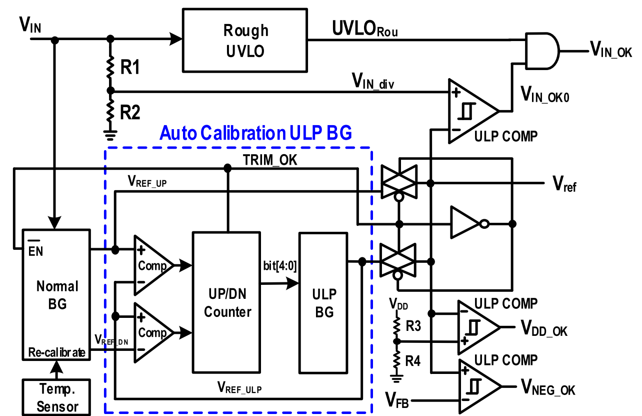

Fig. 20. Architecture of the proposed accurate ULP UVLO.

the GaN driver when there is no input PWM signal, the quiescent current of UVLO needs to be reduced. However, in conventional low-power UVLO [21], the voltage levels are compared with the threshold voltage of the MOSFETs. Due to PVT variations, the threshold voltage of the MOSFETs will widely change and affect the accuracy of the voltage-level detection. The UVLO aims to shut down the power since the power supply is under the reference voltage to reduce the leakage current and power loss. If V_{IN} changes from high to low, as shown in Fig. 21, an accurate UVLO can shut down the gate driver at time t_4. In contrast, without an accurate UVLO, the rough UVLO simply shuts down the gate driver at about time t_5, resulting in the occurrence of power loss between t_4 and t_5, where V_{NEG} is less negative than the device threshold voltage. Thus, the UVLO circuit with low power consumption and high accuracy is needed.

To achieve higher accuracy of voltage detection, the bandgap reference is adopted to generate the reference voltage V_{ref}. Through the low power comparator, V_{ref} is compared with the detected voltage, and the enable signals V_{IN_OK}, V_{DD_OK}, and V_{NEG_OK} will be generated. To avoid error in the comparison results due to low supply voltage V_{IN}, rough UVLO is applied to blank the signals when V_{IN} is smaller than the minimum operation voltage of the comparator. This ensures the accuracy of UVLO output results.

To reduce the quiescent current, the ULP bandgap is used to generate V_{ref}. However, compared to the normal bandgap, the reference voltage of ULP bandgap V_{REF_ULP} is more sensitive to the process variations, which may reduce the accuracy of UVLO. In the proposed structure, the normal bandgap is used to calibrate V_{REF_ULP}. Through the up/down (UP/DN) counter, V_{REF_ULP} can be controlled in the hysteretic window (V_{REF_UP} and V_{REF_DN}) automatically. After the autocalibration of ULP bandgap is complete, the ULP bandgap will take over to generate V_{ref}, and the normal bandgap is turned off to reduce quiescent current. However, temperature variation will seriously affect the performance of GaN HEMT. Thus, a temperature sensor is added to detect the temperature variation. Once the temperature variation is higher than 20 °C, the temperature sensor will send the recalibration request, as shown in Fig. 22, to the UVLO and threshold detection circuit to ensure accurate values.

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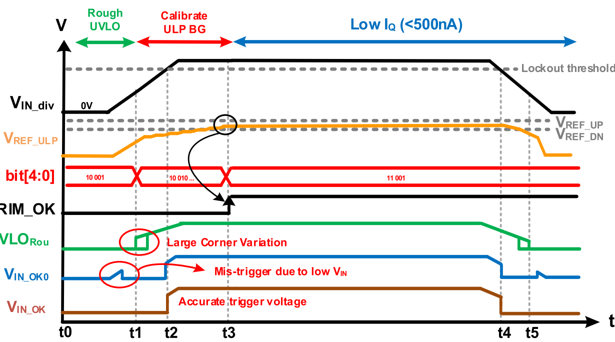

Fig. 21. Operation timing diagram of accurate ULP UVLO.

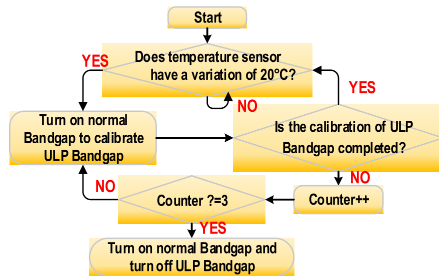

Fig. 22. Recalibration flowchart of an accurate ULP UVLO.

Fig. 21 shows the operation timing diagram of the accurate ULP UVLO. During time period t_0–t_1, the supply voltage V_{IN} is lower than the operation voltage of the comparator. The wrong comparison result occurs at V_{IN_OK0} and is blanked by the signal $UVLO_{Rou}$. At time t_1, $UVLO_{Rou}$ rises to logic high, the divided V_{IN} signal V_{IN_div} is compared with the lockout threshold voltage V_{REF_UP}, which is generated by the normal bandgap, and the calibration of ULP bandgap by the hysteretic window from normal bandgap begins. At time t_2, V_{IN_div} rises above V_{REF_UP}, and V_{IN_OK} rises to logic high to release lockout of V_{IN}. At time t_3, the calibration of ULP bandgap completes, and the ULP bandgap takes over to generate the lockout threshold voltage. Then, the normal bandgap is turned off to reduce the quiescent current. In normal operation, the quiescent current of accurate ULP UVLO can be reduced to less than 500 nA. Finally, the accuracy of the ULP bandgap is 7.1 ppm after the calibration, while the accuracy of the normal bandgap is 3.2 ppm.

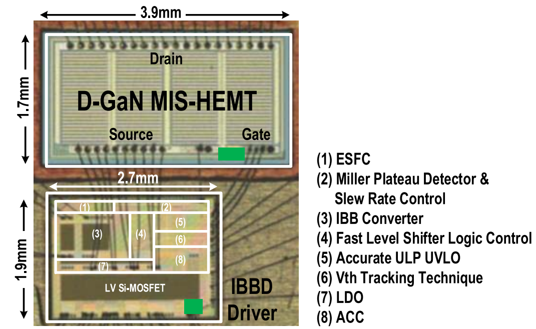

Fig. 23. Chip micrograph with an area of 5.1 and 6.6 mm^2.

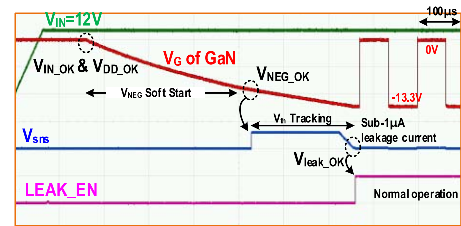

Fig. 24. Measured leakage current with V_{th} tracking process.

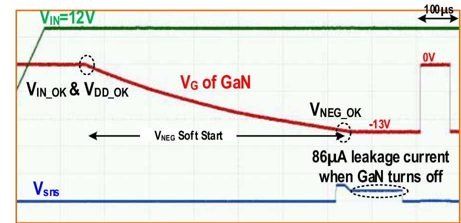

Fig. 25. Measured leakage current without V_{th} tracking process.

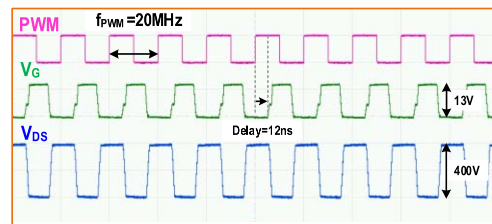

Fig. 26. Measured switching waveform with 20-MHz switching frequency.

IV. Measurement Results

The chip microphotograph is shown in Fig. 23. The proposed IBBD GaN driver with 0.5-μm CMOS process and one 600-V D-GaN MIS-HEMT is integrated by system in package (SiP) with an active area 5.1 and 6.6 mm^2, respectively. The input voltage is 600 V, and the range of switching frequency is up to 20 MHz. In addition, the maximum dV_{DS}/dt SR can reach 120 V/ns.

The measurement of the V_{th} tracking process is shown in Fig. 24. In power on procedure, V_{IN} and V_{DD} are charged to the target level of 12 and 5 V, respectively. Then, $V_{NEG}$is charged to a predetermined value of −10 V in the soft start procedure. When the soft start procedure ends, the V_{th} tracking mode is triggered to calibrate V_{NEG} to −13.3 V, which can fully turn off the switch. Hence, the system can operate normally with a leakage current less than 1 μA. However, without V_{th} tracking, V_{NEG} is set to −13 V, which has a large 86-μA leakage current, as shown in Fig. 25. Fig. 26 shows the measured waveform of V_G and V_{DS} with 20-MHz operation frequency. Due to the fast-level shifters, the rising delay and falling delay in the GaN gate driving signal can be reduced to about only 12 ns.

Fig. 27 shows the measured switching frequency f_{COT} of IBB converter in normal operation mode. Due to the ESFC technique, switching frequency f_{COT} is synchronized with the frequency of PWM signal to further suppress EMI. The ripple of V_{NEG} is within 20 mV when the frequency

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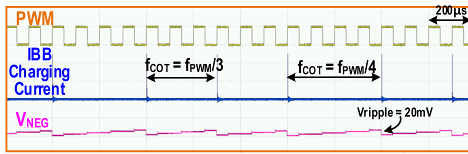


Fig. 27. Measured switching frequency of IBB converter in normal operation mode. f_{COT} synchronizes with f_{PWM}.

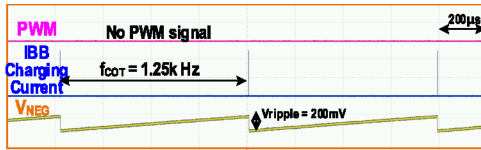


Fig. 28. Measured switching frequency of IBB converter in power saving mode, since PWM disappears and reduced f_{COT} is needed for high efficiency.

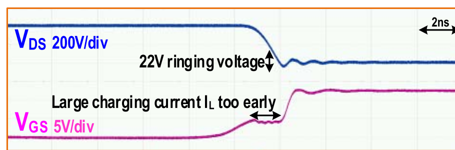


Fig. 29. Measured V_{DS} and V_{GS} without MP detector.

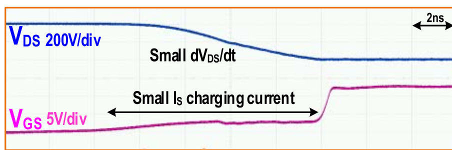


Fig. 30. Measured V_{DS} and V_{GS} with MP detector but without SR control.

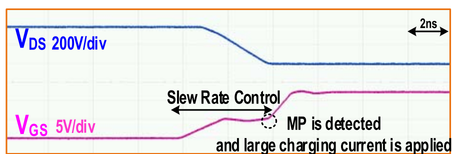
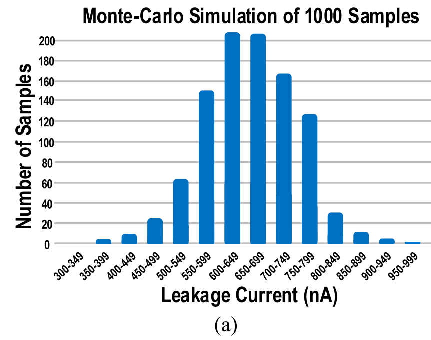


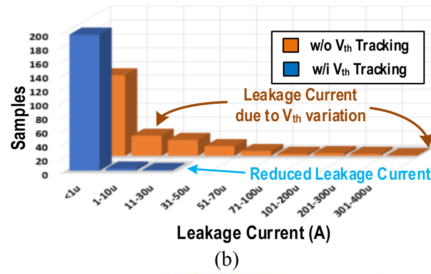
Fig. 31. Measured V_{DS} and V_{GS} with MP detector and SR control.

of PWM signal is 10 kHz. When the system switches into standby mode, the switching frequency of IBB converter will be reduced by power saving mode to enhance light load efficiency. Fig. 28 shows the measured switching frequency f_{COT} of IBB converter in power saving mode, which the switching frequency f_{COT} is reduced to 1.25 kHz and the ripple of V_{NEG} is within 200 mV.

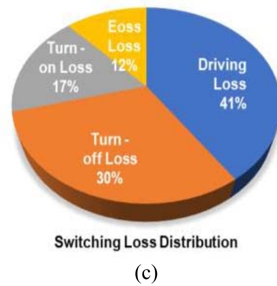
Fig. 29 shows the measured waveform of V_{DS} and V_{GS} of the D-GaN power HEMT without the MP detector. The ringing voltage of 22 V occurs at drain, causing the issue of large EMI. In addition, the measured waveform of V_{DS} and V_{GS} without SR control is also shown in Fig. 30. The low SR of V_{DS} causes the limited switching frequency of PWM signal. With the MP detector and SR control, the ringing voltage of 22 V at drain can be reduced to about 1.9 V, and the SR of V_{DS} can be well-controlled to 120 V/ns, increasing the maximum switching frequency, as shown in Fig. 31.



(a)



(b)



(c)

Fig. 32. (a) Monte Carlo simulation shows that the leakage current can be kept 3σ smaller than 950 nA. (b) Measured leakage current of 400 samples. (c) Pi-chart of switching loss.

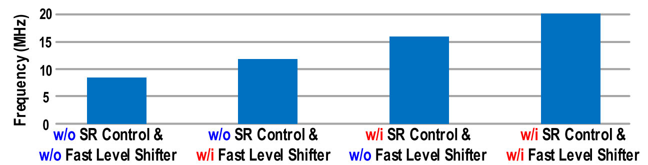


Fig. 33. Maximum switching frequency with and without SR control and fast-level shifter.

Fig. 32(a) shows the Monte Carlo simulation of the leakage current. The leakage current can be kept 3σ smaller than 950 nA. Fig. 32(b) presents the measured leakage current of 400 samples; 200 samples use the V_{th} tracking technique, and the others do not. Without the V_{th} tracking technique, severe leakage current will occur due to V_{th} variation. Therefore, only 75% of the samples have a leakage current below 1 μA. On the other hand, with the V_{th} tracking technique, the leakage current of 98% of the samples is less than 1 μA. Fig. 32(c) shows the pi-chart of switching loss. Fig. 33 shows the maximum switching frequency with and without the SR control and fast-level shifter. Compared with conventional structures, the proposed GaN driver with an SR control and fast-level shifter can reach 2.4$\times$ higher $f_{\mathrm{SW(MAX)}}$ improvement.

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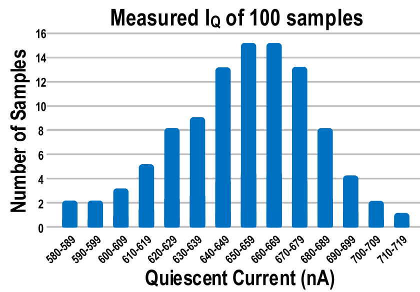

Fig. 34. Measured quiescent current of 100 samples.

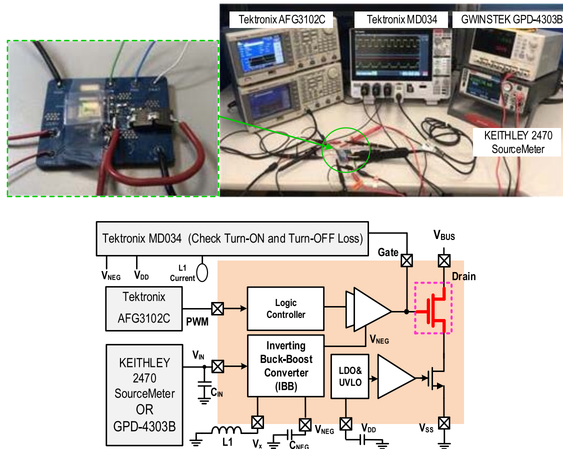

Fig. 35. Experimental setup.

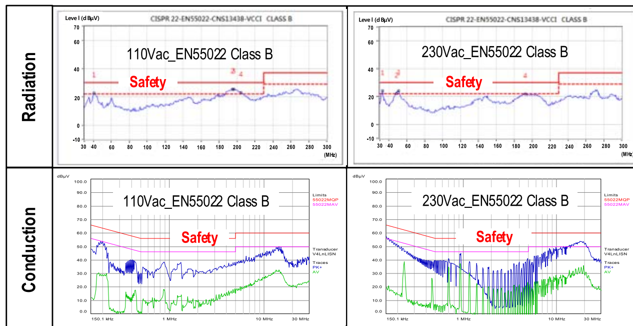

Fig. 36. Measured EMI spectrum passes the EN55022 Class B full-band test.

Fig. 34 shows the measured quiescent current of 100 samples. With the accurate ULP UVLO and the power saving mode in the IBB converter, the quiescent current during no input PWM signal can be reduced to less than 720 nA, and the lowest value achieves 583 nA. Fig. 35 shows the experimental setup.

Fig. 36 shows the EMI measurement result of an adaptor with the proposed IBBD GaN driver, which is tested under 65 W. This shows that when the IBBD GaN driver operates in power saving and PWM synchronization modes, it meets the CISPR-22 Class B standard for the EMI requirement. In the EMI test, EN5502 divides the spectrum into two parts. One is 150 K–30 MHz and the other is 30 M–300 MHz. The proposed PWM synchronization mode can pass the EMI full-band test.

TABLE I
COMPARISON TABLE

	[3] ISSCC17	[4] ISSCC18	[5] ISSCC20	[6] ISSCC21	**This work**
Process	0.35μm HV BCD	0.18μm BCD	GaN	0.5um 600V SOI	**0.5μm CMOS**
Topology	CMOS Driver + E-GaN Switch	CMOS driver + E-GaN Switch	GaN driver + E-GaN Switch	CMOS Driver + E-GaN Switch	**SiP (CMOS Driver + D-MIS GaN)**
Control mode	Adaptive Tri-Slope Gate Driving	Three-Level Gate Driving	Rail-to-Rail Gate driving	Dynamic Feedback Delay Compensation	**V_{th} tracking + MP&SR Control**
V_{th} tracking	No	No	No	No	**Yes**
Operation frequency	10MHz	1.2MHz	26.2kHz	1MHz	**20MHz**
Input Voltage	3V~40V	6V~16V	6.0V	600V	**600V**
Driving Current	1.2A	1.5A	N/A	N/A	**2.5A**
dV_{DS}/dt slew rate	33.3V/nsec*	28.6V/nsec*	N/A	67V/nsec	**120V/nsec**
Power Consumption	39.5mW	N/A	1.33W**	N/A	**6mW**
Efficiency	88.50%	N/A	95.60%	N/A	**95.80%**
Die Size	0.86mm^2	11.27mm^2	2.1mm^2	N/A	**5.1+6.6mm^2**
FoM1 †	746	N/A	N/A	N/A	19160
FoM2 ††	333M	34.32M	N/A	N/A	2400M

*after calculation, **including loss of power converter
† FoM1 = Slew rate * Efficiency / Power consumption
†† FoM2 = Slew rate * Operation frequency

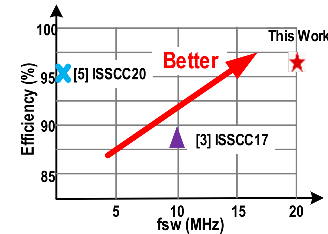

Fig. 37. Operation frequency and efficiency of the proposed technique and state-of-the-arts.

Table I shows the performance comparison table with state-of-the-arts. Through the V_{th} tracking technique, the peak efficiency is improved to 95.8%. Moreover, due to the MP detector and SR control, the maximum switching frequency can be up to 20 MHz and the dV_{DS}/dt can be controlled at 120 V/ns. In comparison with [3], [4], and [6], this work has the highest SR and maximum operation frequency, as shown in Fig. 37.

V. CONCLUSION

The proposed IBBD GaN driver implemented by 0.5-μm CMOS process can drive D-GaN MIS-HEMT directly. Through the V_{th} tracking technique, the leakage current of D-GaN MIS-HEMT can be reduced to sub-1 μA. The MP detector reduces the ringing voltage at drain of GaN switch from 22 to 1.9 V, which succeeds in suppressing EMI. Moreover, the maximum switching frequency can reach up to 20 MHz, and dV_{DS}/dt can be regulated at 120 V/ns by the fast-level shifter and SR control. With the ULP UVLO, the quiescent current can be reduced to 583 nA during standby mode, which enhances the light load efficiency. The peak efficiency is as high as 95.8% and chip areas are 5.1 and 6.6 mm^2.

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